IN THE SPECIFICATION:

Please amend the specification as follows:

1. Amend the paragraph on page 2, lines 16-23, to read as follows:

In FIG. 1, memory 11 outputs vector $\alpha^{i0}$ corresponding to row number i ($0 \leq i < N$) input to exclusive logical sum calculator 13. Memory 12 outputs vector $\alpha^{j}$ corresponding to column number j ($0 \leq j < M$) input to exclusive logical sum calculator 13. Exclusive logical sum calculator 13 calculates an exclusive logical sum of [[$\alpha^{j0}$]] $\alpha^{i0}$ and $\alpha^{j}$ and outputs calculation result $\beta$ to memory 14.

2. Amend the paragraphs on page 9, lines 2-13, to read as follows:

Interleave address generation apparatus 100 shown in FIG. 4 is mainly constructed of counter control section 101, bit inversion ~~apparatus~~ section 102, column ~~conversion apparatus~~ exchange section 103, shift register 104, adder 105 and size comparison section 106.

Furthermore, column ~~conversion apparatus~~ exchange section 103 is mainly constructed of memory 110, memory 111, memory 113 and exclusive logical sum calculator 112.

In FIG. 4, counter control section 101 outputs row number i ($0 \le i < 2^2$) on a two-dimensional array to bit inversion ~~apparatus~~ section 102 and column number j ($0 \le j < 2^3$) on a two-dimensional array to memory 111.

3. Amend the paragraph beginning on page 9, line 27, and ending on page 10, line 9, to read as follows:

Bit inversion ~~apparatus~~ section 102 carries out bit inversion of row number i output from counter control section 101 in a binary state and outputs bit-inverted row number i' to memory 110 and shift register 104. More specifically, bit inversion ~~apparatus~~ section 102 switches between the higher digit and the lower digit of the binary coded row number. That is, bit inversion ~~apparatus~~ section 102 switches the highest digit and lowest digit, then switches between the 2nd highest digit and the 2nd lowest digit. And this same switching between a higher digit and lower digit is continued.

4. Amend the paragraphs beginning on page 10, line 27, and ending on page 11, line 5, to read as follows:

Shift register 104 bit-shifts the value output from bit inversion ~~apparatus~~ section 102 and outputs this to adder 105 as an address offset value.

Adder 105 adds up the output from shift register 104 and the output from column ~~conversion apparatus~~ exchange section 103 and outputs the addition result to size comparison section 106.

5. Amend the paragraph on page 12, lines 9-18, to read as follows:

In FIG. 6, i and j denote a row number and column number output from counter control section 101 and i′ denotes a row number output from bit inversion ~~apparatus~~ section 102. Furthermore, $\alpha^{i0}$ and $\alpha^{j}$ denote vector data output from memory 110 and memory 111 and $\alpha^{i0} + \alpha^{j}$ denotes the calculation result in exclusive logical sum calculator 112. $\mathrm{Log}_{\alpha}\ \alpha^{i0} + \alpha^{j}$ denotes data output from memory 113 and the offset addition result denotes the result of the addition of an offset address output from shift register 104.

6. Amend the paragraph on page 12, lines 21-28, to read as follows:

First, counter control section 101 outputs row number i=0, column number j=0. Bit inversion ~~apparatus~~ section 102 outputs row number i after switching between the higher digit and lower digit of the row number bits in a binary state. Row number i=0 is expressed as "00" in a two-bit binary number and when the

higher bit and lower bit are switched round, the row number is "00" and row number i'=0 is output.

7. Amend the paragraph on page 14, lines 2-10, to read as follows:

As shown above, the interleave address generation apparatus controls so that i is reset every time i exceeds a maximum value and in this way sequentially outputs addresses for a $2^2 \times 2^3$ two-dimensional array in the column direction. Furthermore, the interleave address generation apparatus uses output i' from bit inversion ~~apparatus~~ section 102 as the read address value for memory 110, and can thereby carry out row exchange on the aforementioned two-dimensional array simultaneously.

8. Amend the paragraphs on page 15, lines 10-23, to read as follows:

In FIG. 7, storage cell array 151 temporarily stores row number i' output from bit inversion ~~apparatus~~ section 102 and then outputs row number i' to shift register 104.

For example, storage cell array 151 is constructed of a two-stage storage cell array to adjust the timings of the output from column ~~conversion apparatus~~ exchange section 103 and the

output from shift register 104 to the timing of the output value i' from bit inversion ~~apparatus~~ section 102.

Then, output value i' from bit inversion ~~apparatus~~ section 102 is temporarily stored in storage cell array 151, sequentially output in synchronization with the addition timing of adder 105, input to shift register 104 and a value resulting from shifting 3 bits is output as an address offset value for the i'th row.